- Ordering logistics question
 - Send links directly to Chis
 - Confirm availability
 - Chips, evaluation modules, samples, ASAP first task
 - LNAs finalized already
 - Finalize chip selection, get those eval boards
- Coordination with Chis
- Help with RF circuits

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- (At this point) Select PCB material
 - Microstrip transition line on PCB (char impedance, 50 ohms)
 - Proportionality of width of strip, height of substrate, and dielectric constant of PCB material
- ADS: linecalc is application within it
 - MLIN
 - Yields known width for lines
 - "Controlled impedance line"
- Stackup: another important consideration
 - RF
 - RF ground
 - RF doesn't see anything below the RF ground layer, fields confined there
 - Induced current density on ground plane
 - Just has to be a big chunk of metal, could be power, gnd, or split plane
 - What you don't want:



- It'll cause a lot of reflections and noise

Retired stackup (H, Er) Route lines with W Key a clay REGND

- 3) keep a clear RF ground below it
- 4) Use a low loss epsilon R
 - No FR4 (can't go past a couple MHz)
 - Rogers 4350B, 4003C, etc.
 - Chisum will help us find board manufacturer
- Top layer has all RF circuit stuff (block diagram: BFIC, LNAs, etc). Then, via down
- SPI bus comes up to talk to BFIC and LO thru via
- Chisum's timeline
 - Finalize design late next week
 - Leaning toward: swept local oscillator, DC power for each 1 MHz
 - Question: what is bandwidth we want to sweep over? What is chanel width?
 - Expl of circuit block diagram we talked about on Monday
- Eval board for chips we already know about (like LO, LNA, BFIC?)
 - Hook em up with coax & get code working with whole system pre-chip
 - Xmicrowave blocks that chis already has, probs for LO, IQ demod, BFIC
 - Finalizing process means picking chip & finding eval boards



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- 24GHz electronics that we're operating at 22GHz, final choice to operate at 24 would only be antenna layout stuff